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Complete If Known			
Application Number	09/841,974		
Filing Date	4/24/01		
First Named Inventor	Terry Lee Goode		
Art Unit	2128		
Examiner Name	Fred O. Ferris III		
Attomey Docket Number	003921.00011		

	U.S. PATENT DOCUMENTS					
Examiner Cite thitiats No.	Document Number Publication (Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant		
		Number - Kind Code ² (if known)			Figures Appear	
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Examiner Cite No.1	Cite	Foreign Patent Document	Publication	Name of Patentee or	Pages, Columns, Lines,	
	Country Code ⁸ - Number ⁸ - Kind Code ⁸ (if known)	Date MM-DD-YYYY	Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear	T ⁶	
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1.		GB 1,444,084	07-28-1976	Cheesman		
7		GB 2,182,220	05-07-1987	Austin		
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Examiner Signature	212	Date Considered	8/7/05	
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ADDINGS TO STATION INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known Application Number 09/841.974 Filing Date 4/24/01 First Named Inventor **Terry Lee Goode** 2128 Art Unit Fred O. Ferris III Examiner Name Attorney Docket Number 003921.00011

(Use as many sheets as necessary)

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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
Z		Kronstadt, et al., "Software Support for the Yorktown Simulation Engine," 19th Design Automation Conference, Paper 7.3, 1982, pp. 60-64			
2		Kolke, et al., "HAL: A High-Speed Logic Simulation Machine," IEEE Design & Test, Oct. 1985, pp. 61-73			
Z		Shear, "Tools Help you Retain the Advantages of Using Breadboards in Gate-Array Design," EDN, Mar. 18, 1987, pp. 81-88			
3		J.W. Babb, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulation," Masters Thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, Nov. 1993; Also available as MIT/LCS Technical Report TR-686			
ξ		M. Dahi, J. Babb, R. Tessier, S. Hanono, D. Hoki, and A. Agarwal, "Emulation of the Sparcle Microprocessor with the MiT Virtual Wires Emulation System, " IEEE Workshop on FPGAs for Custom Computing Machines '94 (FCCM '94), Apr. 1994			
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Examiner Signature	12	Date Considered	8(7	105

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